



## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

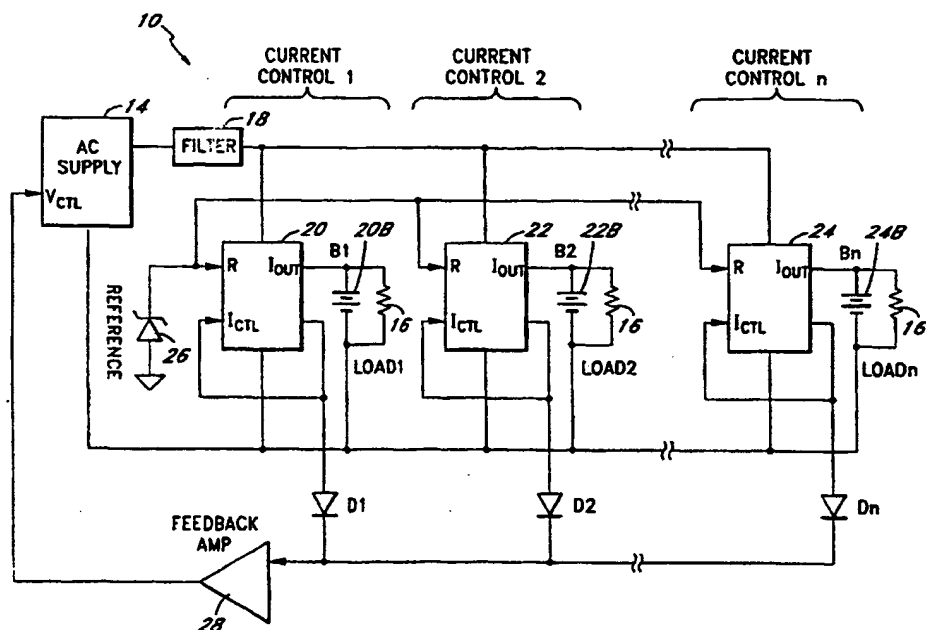
(51) International Patent Classification <sup>5</sup> : <b>H02J 7/00</b>	<b>A1</b>	(11) International Publication Number: <b>WO 95/00992</b> (43) International Publication Date: <b>5 January 1995 (05.01.95)</b>
(21) International Application Number: <b>PCT/US94/07032</b> (22) International Filing Date: <b>21 June 1994 (21.06.94)</b> (30) Priority Data: 08/080,272                      21 June 1993 (21.06.93)                      US (71) Applicant: <b>AST RESEARCH, INC. [US/US]; 16215 Alton Parkway, Irvine, CA 92718 (US).</b> (72) Inventor: <b>BRAINARD, Gerald, L.; 1366 Stephen Way, San Jose, CA 95129 (US).</b> (74) Agent: <b>SEWELL, Jerry, T.; Knobbe, Martens, Olson and Bear, 16th floor, 620 Newport Center Drive, Newport Beach, CA 92660 (US).</b>		(81) Designated States: <b>AU, CA, CN, JP, KR, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).</b>  <b>Published</b> <i>With international search report.</i>

(54) Title: **MAXIMALLY EFFICIENT MULTIPLE BATTERY RAPID CHARGER/COMPUTING DEVICE POWER CONTROLLER**

## (57) Abstract

A battery charging system (10) includes an efficient switch mode power supply (14), multiple linear current limiters (20, 22, 24; 122, 123, 124), and a feedback circuit (28) to allow the switch mode power supply (14) to operate at the minimum voltage necessary to operate a power load and charge batteries (20B, 22B, 24B). Furthermore, the switch mode power supply (14) is capable of producing the maximum power required by the system (10), such as when the battery charger is used in conjunction with operation of an electronic device with peak load demands such as when a hard disk is accessed in a portable computer. Two control mechanisms are found in the battery charging system.

The first mechanism is an input used to control the switch mode power supply output voltage from an external source. In one embodiment, this is done by referencing a first voltage to that internal to the switch mode power supply (14). The second mechanism is to limit the current within the switch mode power supply (14) not controlled by an external source. This current-limiting feature is linear and is set at an absolute limit point. Each limiter (20, 22, 24; 122, 123, 124) supplies charge current to a battery (20B, 22B, 24B), which charge current is monitored and compared to a reference voltage from a reference voltage source (132) with the resulting error voltage used to control the output of a series pass controller, such as a transistor (Q3, Q5, Q7).



**FOR THE PURPOSES OF INFORMATION ONLY**

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	GB	United Kingdom	MR	Mauritania
AU	Australia	GE	Georgia	MW	Malawi
BB	Barbados	GN	Guinea	NE	Niger
BE	Belgium	GR	Greece	NL	Netherlands
BF	Burkina Faso	HU	Hungary	NO	Norway
BG	Bulgaria	IE	Ireland	NZ	New Zealand
BJ	Benin	IT	Italy	PL	Poland
BR	Brazil	JP	Japan	PT	Portugal
BY	Belarus	KE	Kenya	RO	Romania
CA	Canada	KG	Kyrgyzstan	RU	Russian Federation
CF	Central African Republic	KP	Democratic People's Republic of Korea	SD	Sudan
CG	Congo	KR	Republic of Korea	SE	Sweden
CH	Switzerland	KZ	Kazakhstan	SI	Slovenia
CI	Côte d'Ivoire	LI	Liechtenstein	SK	Slovakia
CM	Cameroon	LK	Sri Lanka	SN	Senegal
CN	China	LU	Luxembourg	TD	Chad
CS	Czechoslovakia	LV	Latvia	TG	Togo
CZ	Czech Republic	MC	Monaco	TJ	Tajikistan
DE	Germany	MD	Republic of Moldova	TT	Trinidad and Tobago
DK	Denmark	MG	Madagascar	UA	Ukraine
ES	Spain	ML	Mali	US	United States of America
FI	Finland	MN	Mongolia	UZ	Uzbekistan
FR	France			VN	Viet Nam
GA	Gabon				

-1-

## MAXIMALLY EFFICIENT MULTIPLE BATTERY RAPID CHARGER/COMPUTING DEVICE POWER CONTROLLER

### Background of the Invention

5 The present invention is directed towards an efficient battery charger, and more specifically, to an efficient multiple battery charger having an improved power controller that senses the power demand on each battery and provides the minimum output voltage required to charge all, including the battery with greatest demand.

10 In battery powered portable electronic systems the portable power supply is usually provided by either disposable batteries, replaceable batteries, such as Nickel Cadmium (Ni-Cd), or other rechargeable batteries. The disposable batteries are well known, but are not rechargeable. Since many users desire to use their electronic device without regard to whether an electrical outlet is available to power the device, such consumers typically rely on rechargeable batteries to power the device. One such type of battery is the rechargeable battery, which typically requires a dedicated battery  
15 charger. Another type of battery is a battery pack specifically designed for the portable electronic device. In this type of device, the manufacturer of the device allows the battery pack to be replaceable so that a second battery source can be carried to replace the first pack in the event that the first battery pack has its charge depleted. The next type of batteries are those intended to be permanently installed in the device. Once the  
20 batteries are drained of their energy, either they must be recharged or the device must be powered by an alternative power source before the device can resume operation.

In devices that use either separate battery power packs or internal batteries, several batteries are charged during the same recharging session. Most frequently, each battery is at a different voltage level from the others in the pack. This leads to an  
25 inefficient charging scheme when all batteries are being recharged simultaneously. Alternatively, some systems attempt to recharge each battery separately from the others, but do so in a manner that is highly inefficient in that the charging load does not adjust as the voltage charge on each battery reaches a full charge state. This power loss is

-2-

usually in the form of heat, which can be damaging to the electronic device if any of the fail safe mechanisms in the device fail under certain circumstances.

Accordingly, what is needed is a battery charger with a power controller that operates at the minimum voltage possible in order to reduce power loss and heat.

5 Furthermore, the power charger should be able to respond to peak loads when used in combination with the powering of the electronic device while charging the batteries to operate the device without interfering with system performance.

#### Summary of the Invention

10 According to the invention, a battery charging system is disclosed using a power supply, such as a switch mode power supply, and multiple linear current limiters. The limiters use feedback means associated with the battery charger to allow the switch mode power supply to operate at the minimum voltage necessary to operate a power load and charge batteries. This system also allows the switch mode power supply to produce maximum power required by the system. Such maximum power production  
15 occurs when the battery charger is used during the same time as the operation of an electronic device with peak load demands, such as when a hard disk is accessed in a portable computer.

The battery system further includes two control mechanisms for increasing operating efficiency. The first mechanism is an input for controlling the switch mode  
20 power supply output voltage from an external source. In one embodiment, this is done by referencing a first voltage to the voltage internal to the switch mode power supply. The second mechanism limits the current within the switch mode power supply not controlled by an external source. This current limiting feature is linear and is set at an absolute limit point. Each limiter supplies charge current to a battery, which charge  
25 current is monitored and compared to a reference voltage with the resulting error voltage used to control the output of a series pass controller, such as a transistor.

### Brief Description of the Drawings

Figure 1 is a block diagram of a battery charger according to the present invention, which is able to charge multiple batteries at the minimum voltage possible; and

5           Figures 2A, 2B and 2C are schematic diagrams illustrating the specific embodiment of the battery charger in Figure 1.

### Detailed Description of Specific Embodiments

A battery charger 10 with an efficient power controller 12 is disclosed in Figure 1 and described below. Battery charger 10 includes a power source 14, typically an  
10           alternating current voltage source such as, for example, the 110 AC voltage from any electrical outlet common to most buildings. The power source 14 modifies and rectifies the voltage and then steps it down to a level useable by the battery charger 10 and, subsequently, the load 16 to be powered. These techniques are well known in the art and are left to the skilled artisan for implementation. The power source may also be  
15           the type used and described in, for example, commonly assigned U.S. Patent Application No. 08/080,384, titled Universal Power Converter, filed on June 21, 1993. The power source 14 is further connected to a noise filter 18, which is used to filter the power supplied to the battery charger 10 and load 16.

The power source is further connected to various current control circuits 20, 22  
20           and 24, which are used to regulate the current, thus limiting the voltage applied to their respective batteries, 20B, 22B and 24B. Each of the current control circuits 20, 22 and 24 is further connected to their respective battery 20B, 22B and 24B. According to the present invention, the number of control circuits is determined by the number of battery packs, which can be any number N. One current control circuit is provided for each  
25           battery pack. Each battery 20B, 22B and 24B is further connected to the load 16, such as, for example, a personal portable computer, a cellular phone, a portable stereo, or any other like electronic device.

-4-

Furthermore, the batteries may use non-dissipative charge equalization controls as, for example, described in commonly assigned U.S. Patent Application No. 08/080,898, titled Non-Dissipative Battery Charger Equalizer, filed on June 21, 1993.

5 Finally, the power source 14 is further connected to a voltage reference 26, which is used to control the current in each current control circuit 20, 22 and 24 and subsequently to control the voltage applied to each battery as charged.

10 The power supply 14 intended for use in the battery charger 10 is based on a switch mode power supply and is used in conjunction with multiple linear current limiters, which are implemented in the current control circuits 20, 22 and 24. Feedback amplifier 28 is used in conjunction with the current limiters to operate the switch mode power supply in such a manner as to minimize the voltage output for charging the batteries or operating the system. The switch mode power supply is capable of producing a maximum power required by the system. This system uses two control mechanisms. The first is an input used to control the switch mode power supply output voltage from an external source. This is typically in the form of a voltage that is compared with a reference internal to the switch mode power supply. The second mechanism is current limiting within the switch mode supply not controlled by an external source. The current limiting is linear and is set at an absolute limit point. Other types of current limiting are not intended to be used, which types include hold back or burp mode limiting. Importantly, the switch mode power supply must operate reliably in either the voltage or current modes. This is accomplished by causing the switch mode power supply to current limit in a linear fashion.

20 Each current limiter module then supplies the charge current to its respective battery. The charge current is monitored and compared to a reference and the resulting error voltage is used to control the output of a series pass element, which obtains its voltage from the switch mode power supply. Each battery and current sense device may have in parallel a computing device or other electrically powered component and, therefore, the series pass element must be capable of supplying the total of component and battery charging current.

-5-

Several current limiting circuits, or current control circuits may be driven in parallel from a single switch mode power supply. Since any of the batteries can be charging at a voltage different than the others at any given point in time, the switch mode power supply needs to develop sufficient voltage to allow charging the battery with the highest voltage. To reduce power loss and heat in the series pass elements, and to keep such losses at a minimum, the switch mode power supply output is not allowed to be greater than the highest voltage required. Each current source control circuit then has a secondary output that is combined with the other signals in such a way that the one with the greatest signal causing that pass element to be saturated is fed back to the switch mode power supply, thereby causing the power supply to reduce its output to maintain the correct charge current for that battery. By this means, there is always one of several series pass elements that is fully saturated, insuring that the output of the switch mode power supply will be no greater than the minimum required.

Based on this arrangement, during moments of peak loading, such as spinning up a hard disk, a CD-ROM drive, or any other like peak load operation, the switch mode power supply is not required to continue full rapid charging on all batteries and reduces its output below that which will sustain rapid charge in all batteries, which action is accomplished by the internal current limiter. This diverts the current necessary to supply the power to the demand load momentarily.

A preferred embodiment of the present invention is illustrated in Figure 2, which includes Figures 2A, 2B and 2C. In Figures 2A and 2B, the battery charger 110 is connected to a power source, or power supply (not shown), which offers two levels of power for use in the battery charger 110. The first level of power comes in on power main line 128. The second comes in on power auxiliary line 130. The main power line 128 supplies around three (3) Amperes (A) of current, while the auxiliary power line 130 supplies 168 mA. The main power line 128 services the current control circuits 122, 123, and 124 for recharging the batteries (not shown). The auxiliary power line 130 provides operating current for the current control circuitry and substantially follows the main input voltage level.

-6-

A voltage reference element 132, which is powered by the auxiliary power line, provides a stable 2.5 volt reference voltage at the cathode of the Schottky Diode U5. This voltage is divided by resistor pairs R4-R5, R8-R9 and R12-R13, for current control circuits 122, 123 and 124, respectively. The reduced referenced voltage from each voltage divider pair R4-R5, R8-R9 and R12-R13 is then presented to the inverting inputs of amplifiers U1, U2 and U3, respectively. Divider resistors R5, R9 and R13 are grounded remotely to the respective battery pack negative terminals, to reduce the effects of current on the power ground circuit. Each current control circuit 122, 123 and 124 is connected to a respective battery pack (see Figure 2C) wherein a current output line (OUT) 136A, 136B and 136C, a current sense (I.SENS) line 138A, 138B and 138C, a control sense (C.SENS) line 134A, 134B and 134C, and a ground (GND) line 140A, 140B and 140C, are coupled to the battery pack.

In Figure 2C, the battery 220 in the battery pack 120 is connected between the OUT line 136 and the current sense lines, while a regulating resistor 222 is connected in series with the battery 220 and between the I.SENS. line 138 and the C.SENS. line 134. Thus, the battery 220 and resistor 222 are connected between the OUTput line 136 and the I.SENS. and GND. lines 138 and 140, respectively. A resistive load RLOAD, such as a microprocessor of a portable computing device, may be connected in parallel to the battery pack 120.

As illustrated in Figures 2A, 2B and 2C, the C.SENS. lines 134A, 134B and 134C are connected to noninverting inputs of each of the current sense amplifiers U1, U2 and U3, respectively. Current through a given battery is then represented as a voltage at the noninverting input of the corresponding current sense amplifier U1, U2 or U3. The sensed voltage is then compared with the divided reference voltage to cause the amplifier output to respond in a manner that will control the current through the battery.

Current to the batteries is supplied through pass transistors Q3, Q5 and Q7, which are P-channel MOS field effect transistors (FET), and are connected to the main power line 128 on the source side of the transistor and to the battery on the drain side of the transistor, with the gate being coupled to the output of the current sense



-7-

amplifiers U1, U2 and U3, respectively. Charging current is controlled by varying the gate voltage to the pass transistor Q3, Q5 and Q7 from the outputs of the current sense amplifiers U1, U2 and U3, respectively, through current shut off transistors Q2, Q4 and Q6, respectively. Each current shut off transistor Q2, Q4 and Q6, respectively, is  
5 turned off during the absence of input power to prevent the batteries from discharging through resistors R6, R10 and R14, respectively, which resistors are current pull up resistors between the respective gate and source of each pass transistor Q3, Q5 and Q7.

Since the pass transistors Q3, Q5 and Q7 are P-channel MOSFETs, they increase conduction as the gate voltage is made to go increasingly negative with respect to the  
10 FET source. As the proper charging current is reached, the output of each current sense amplifier U1, U2 and U3 then increases to provide a gate voltage that maintains the desired current.

A buffer amplifier U4 provides an output voltage to control the main input voltage for each current control circuit 122, 123 and 124. The connection to amplifier  
15 U4 is the power to amplifiers U1-U4. As the output voltage decreases, the main supply output voltage is caused to increase. The output of buffer amplifier U4 is controlled by the lowest signal of all the output signals from current sense amplifiers U1, U2 and U3 through their respective diodes CR1, CR2 and CR3. The input to buffer amplifier U4 is biased by resistor R15.

20 During charging operation, the battery having the highest initial charge will demand the greatest charging voltage. This demand causes the output of its respective error amplifier to decrease in an effort to increase the output of the corresponding pass transistor Q3, Q5 or Q7. This causes a response at the output of buffer amplifier U4 to force the main power supply line 128 to provide the required voltage to the input of  
25 the pass transistor Q3, Q5 or Q7 associated with the battery having the greatest charging voltage demand. In this manner, the pass transistor associated with the battery having the greatest charging voltage demand becomes fully saturated. Via this means, the charging voltage supplied to the controller is held at the minimum voltage required to charge all batteries, thereby reducing the power loss in the main supply and the  
30 charge control pass transistors to a minimum. Each current control circuit 122, 123 and

124 further includes a stabilizing or integrating capacitor C3, C4 and C5, respectively. Furthermore, resistor R15 serves as a bias resistor for each control diode CR1, CR2 and CR3. In addition, resistor R16 provides a 2.5 volt reference to ground at voltage reference U5. Resistor R17 is connected between the auxiliary power line and the voltage reference U5 to provide operating current for the 2.5 volts reference.

Because of the large power handling capabilities of pass transistors Q3, Q5 and Q7, each is mounted on a heat sink to help dissipate the heat generated inside the transistor. It should be noted that the circuitry used in this battery charger control circuit may be implemented in a single integrated chip. Such a chip may be mounted on a single heat sink. On the other hand, the pass transistors may be integrated together on the same chip but separate from the other elements in each current control circuit. This allows the pass transistors to be mounted to the same heat sink.

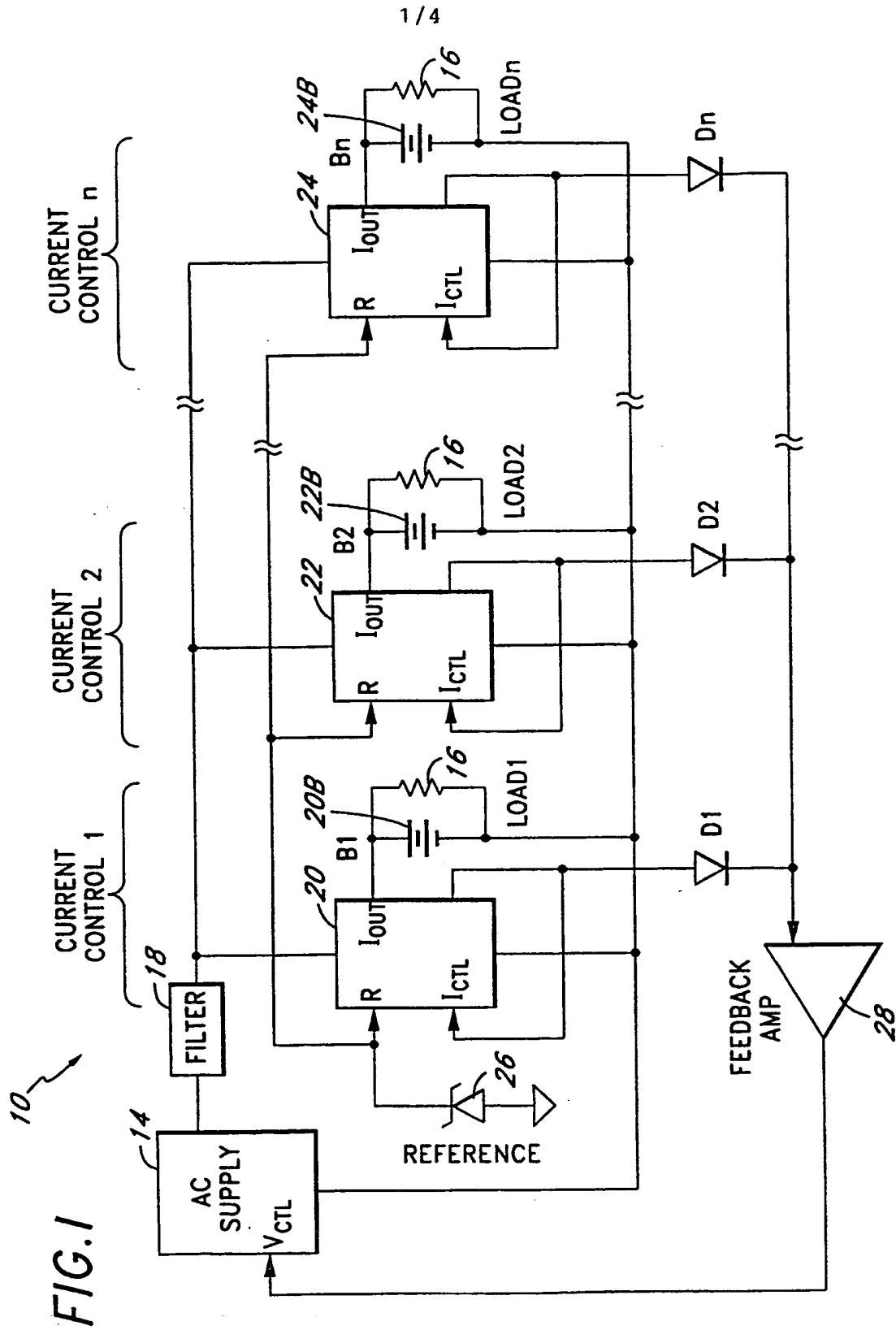
The power dissipated by the series pass elements (charger) depends on charging/load current multiplied by the voltage across the element. Since current is constant (except for trickle charge), power loss is proportional to series pass voltage. Since minimum series pass voltage is maintained, the worst case power loss quickly becomes quite small as battery voltages equalize. As batteries go into trickle charge, power loss becomes negligible. As batteries become similar in voltage and as each battery reaches a full charge, power dissipation is held at a minimum and is eventually reduced to only that necessary to charge the remaining batteries. Once the batteries are fully charged, a trickle charge of only 45 milliwatts is required to maintain the batteries at a full charge state while the power or battery charger is in operation. In typical battery charging systems, the power dissipation does not reduce gradually in a manner that tracks the power requirements to charge the batteries efficiently, rather, the power dissipation is either at full level, for example, 11 watts, or at a trickle charge state of, for example, 45 milliwatts, with no power variation in between. Accordingly, it is apparent that there is a large amount of power loss associated with the prior battery charging systems that are either on full power or at a trickle charge without any power tracking capabilities as the batteries go from reduced power consumption a full depletion state and full charge state.

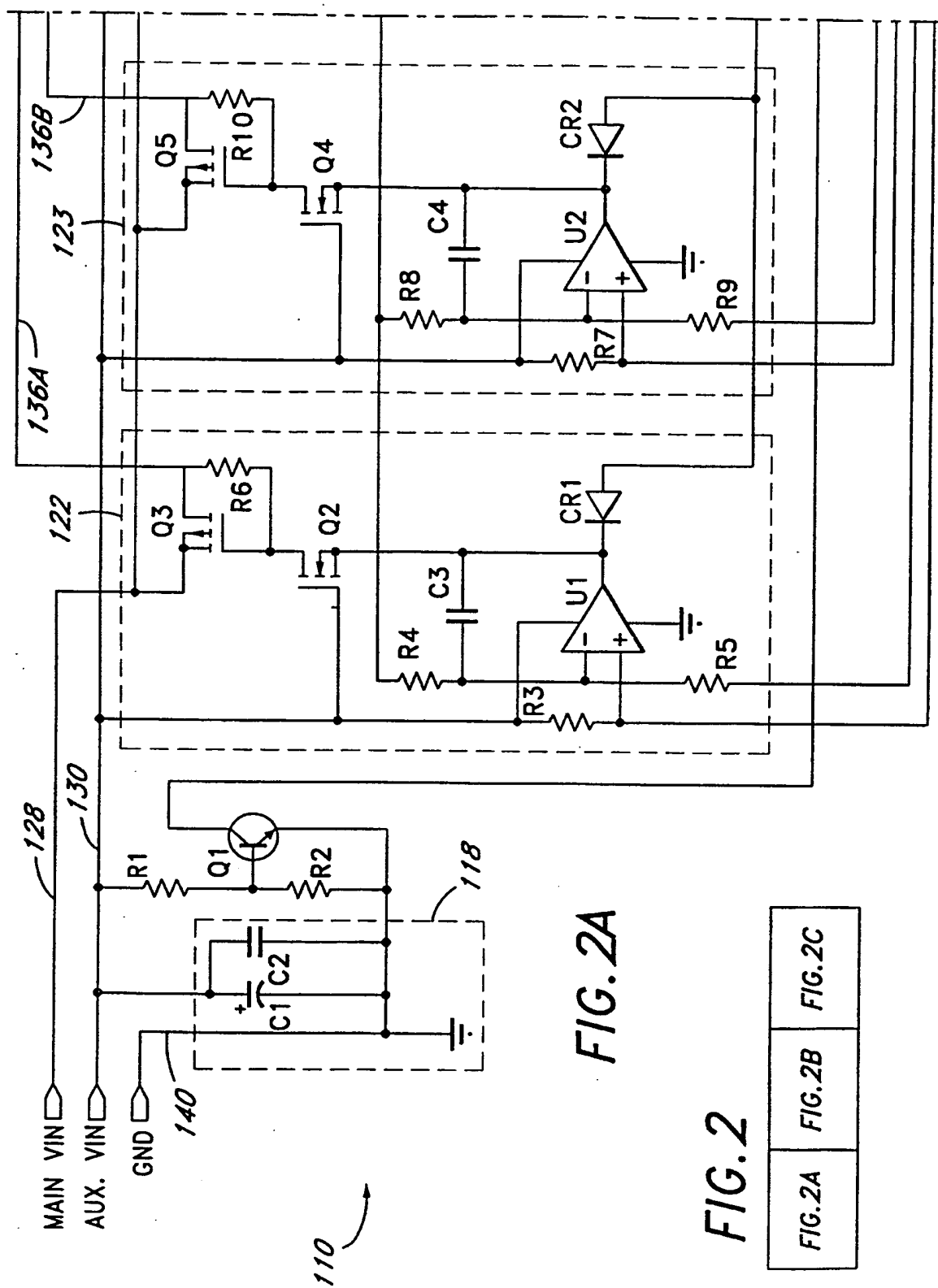
Since the auxiliary power line is used to provide operating current to the current control circuits, a noise filter 118 is provided to filter the voltage before reaching the current control circuits 122, 123 and 124. The noise filter 118 includes a pair of capacitors C1 and C2, which are optimized to provide the best noise filtering capabilities. These two capacitors are connected together in parallel between the auxiliary power line 130 and ground 140. A transistor Q1 is connected between the auxiliary power line 130 and the power enable line 142 of the power supply, which line 142 is used to turn on monitoring circuits in the battery packs when power is available.

A novel battery charging system for charging multiple batteries has been described. It will be understood by those skilled in the art that variations and modifications can be effected within the spirit and scope of the invention as described above and as defined in the following claims.

WHAT IS CLAIMED IS:

1. A battery charging apparatus for charging multiple batteries, characterized  
by:  
a power supply;  
5 a plurality of linear current limiters coupled to said power supply and  
each linear current limiter further connected to a respective battery; and  
means, coupled to said power supply and said plurality of linear current  
limiters, for providing current charging feedback information to said plurality of  
current limiters thus enabling each of said plurality of linear current limiters to  
10 reduce the voltage placed across itself in response to its respective battery charge  
level during charging.
2. The apparatus of Claim 1 wherein said power supply is a switch mode  
power supply.
3. The apparatus of Claim 1 wherein each of said plurality of linear current  
15 limiters comprises a series pass transistor coupled between said power supply and said  
battery for controlling the voltage applied to said battery.





**FIG. 2A**

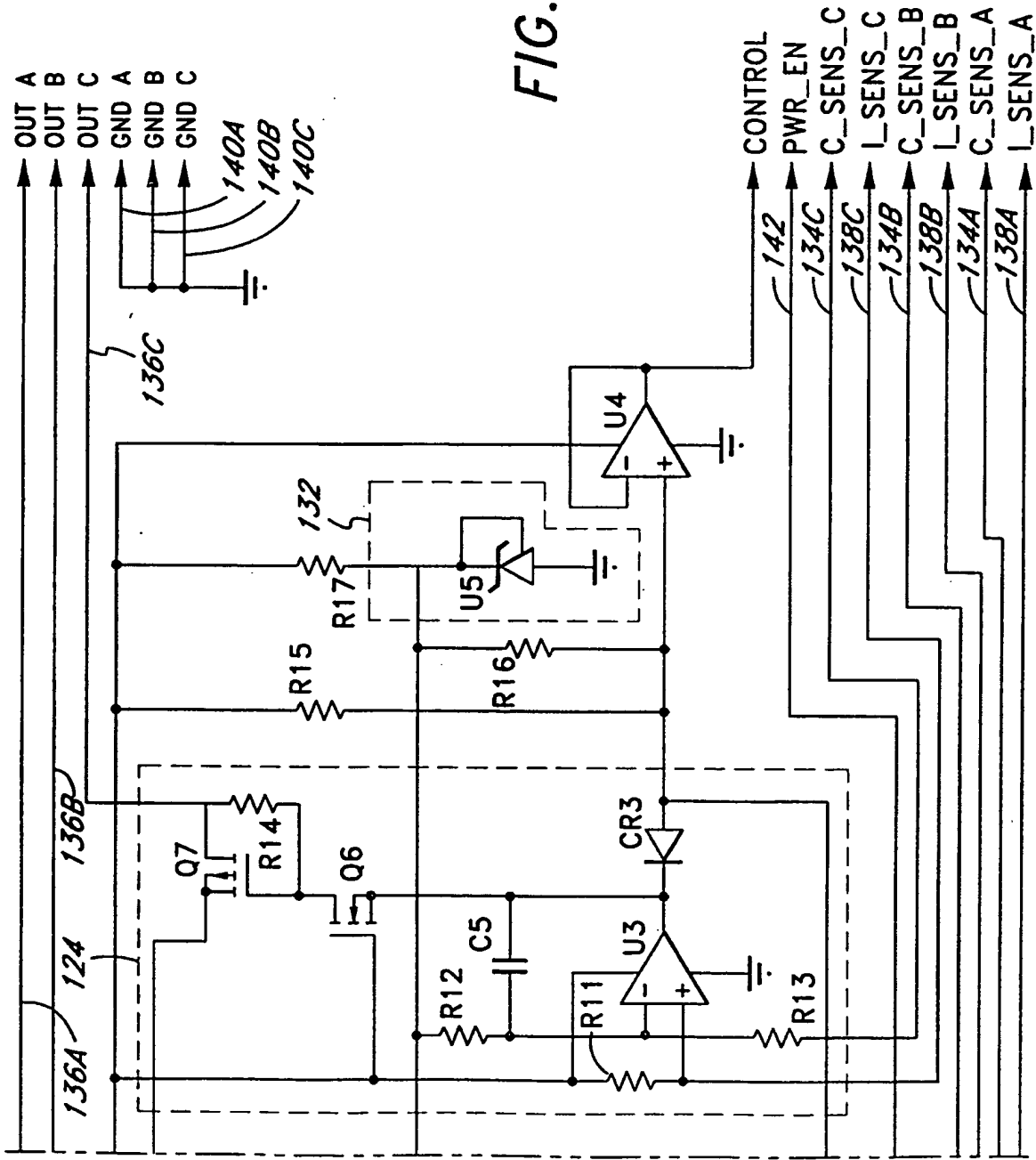
**FIG. 2**

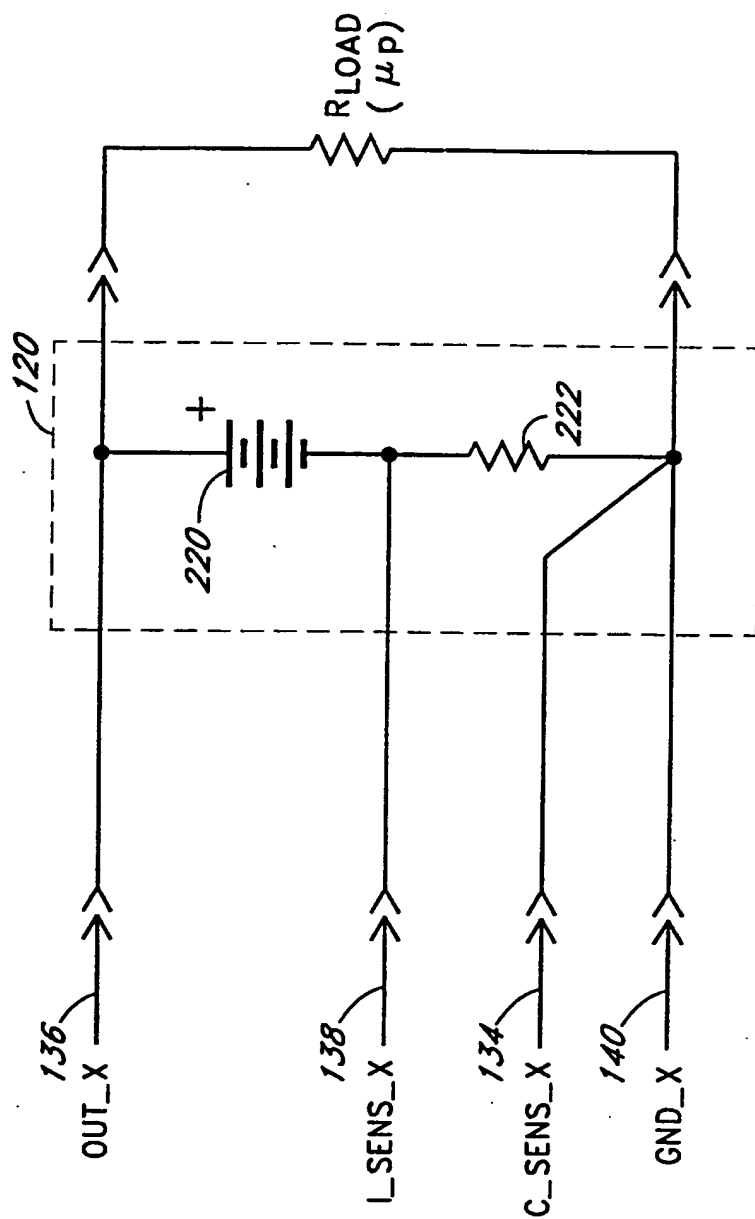
**FIG. 2A**

**FIG. 2B**

**FIG. 2C**

FIG. 2B





**FIG. 2C**



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US94/07032

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(5) :H02 J 7/00

US CL :320/015

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 320/2, 15

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y  A	US, A, 4,849,682 (BAUER et al) 18 July 1989 (see fig. 1 & col. 3, lines 3-20)  US, A. 4,670,703 (WILLIAMS) 02 June 1987 (see fig. 1)	1,2 ---- 3  1-3



Further documents are listed in the continuation of Box C.



See patent family annex.

## \* Special categories of cited documents:

\*A\* document defining the general state of the art which is not considered to be of particular relevance

\*E\* earlier document published on or after the international filing date

\*L\* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

\*O\* document referring to an oral disclosure, use, exhibition or other means

\*P\* document published prior to the international filing date but later than the priority date claimed

\*T\*

later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

\*X\*

document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

\*Y\*

document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

\*Z\*

document member of the same patent family

Date of the actual completion of the international search

23 AUGUST 1994

Date of mailing of the international search report

SEP 06 1994

Name and mailing address of the ISA/US  
Commissioner of Patents and Trademarks  
Box PCT  
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

ROBERT HICKEY

Telephone No. (703) 305-9646